

verification HORIZONS

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With Vision and Planning, You Can Actually Enjoy Upgrading Your Process. Seriously.

By Tom Fitzpatrick, Editor and Verification Technologist

We're finally doing it. My wife and I have been in our house for 13½ years and we're finally redoing our kitchen, which my wife has wanted to do for about 11 years now. This is kind of a big step for us, as those of you who have gone through the exercise can attest, I'm sure. When we had the house built, we chose to limit our budget to keep "expensive" from turning into "exorbitant," and we've been living with formica countertops and a linoleum floor ever since. It's rather exciting seeing the first steps of converting these into granite and hardwood. As you might imagine, I find myself thinking of how this relates to upgrading a verification methodology because I'm sure that, by now, you know that that's how my mind works.

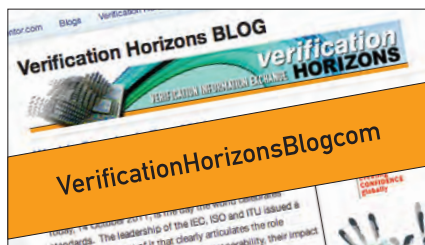
When a project like this comes up, my wife and I work well together. I tend to go overboard and want to buy new appliances, add new cabinets and maybe even throw in a new "island" with a sink. Dee, on the other hand, is the more practical one so we'll be keeping the appliances and cabinets. We are also removing the wallpaper and having the walls painted. So, we've got some "legacy IP" we need to work with, but we'll be able to integrate it all with the new stuff and have a much more useful – and modern – kitchen than we had before. Keep this analogy in mind as you read the following articles.

Our feature article this time comes from my friend Andy Meyer, a fellow Verification Technologist here at Mentor. In "Graph-Based IP Verification in an ARM SoC Environment," Andy shows how the use of graph-based verification methods not only serve to upgrade the quality of your block-level verification efforts, but also how combining graphs with your UVM environment makes it easier to extend block-level components into an SoC test environment. As you'll see, this approach lets you reuse your block-level verification IP both to ensure that your design blocks are functioning properly in the SoC and also easily construct a complex SoC verification environment from the block-level components.



"I find myself thinking of how this (kitchen upgrade) relates to upgrading a verification methodology because I'm sure that, by now, you know that that's how my mind works."

—Tom Fitzpatrick



Our next article comes from Infineon who share their thoughts on how to *“Use Scripting Language in Combination with the Verification Testbench to Define Powerful Test Cases.”* This article shows how to use Tcl (or any scripting language) to simplify the task for designers of customizing testbenches. The article discusses both VHDL and OVM testbenches, but the technique is applicable to UVM as well.

When I was in college, I recall my dad, who was an analog designer, telling me that “it’s an analog world” and that my digital exploits would eventually run into this reality. The truth of my dad’s wisdom is evident in our next article, in which *“STMicroelectronics Engineers Find Mixed Analog-Digital Verification Success with OVM and Mentor Graphics Questa ADMS Simulator.”* In it, you’ll see how STMicro created analog-friendly OVM verification IP that allowed them to take advantage of OVM in generating realistic analog traffic via Questa ADMS.

We next share a couple of “how to” articles on some of the finer points of OVM/UVM testbench design. The first, *“Polymorphic Interfaces: An Alternative for SystemVerilog Interfaces,”* by my colleague Shashi Bhutada, builds on prior work that explores the use of abstract classes to replace virtual interfaces for connecting your OVM/UVM testbench to the DUT. This particular application shows how this technique allows you to create a single driver class that can use different specializations of an interface without having to rewrite anything. This is followed by our monthly article from the UVM/OVM Online Verification Methodology Cookbook at the Verification Academy. This article shows how to set up a UVM environment for verifying layered protocols.

In the Partners’ Corner for this issue, our friends from Test and Verification Solutions share their experiences in helping Dialog Semiconductor to adopt OVM for their verification solution. *“Successful Adoption of OVM and What We Learned Along the Way”* will give you some insight into what you may expect if you’re thinking of doing the same.

Last, but not least, my colleague Darron May asks the important question, *“Process Management: Are You Driving in the Dark with Faulty Headlights?”* This article builds on Darron’s previous article about Questa’s Unified Coverage Database to show how we’ve developed additional technologies in our Verification Management tool to turn the data in the UCDB into valuable information for you to measure and manage your verification process.

I’m concluding this welcome message in my kitchen. The new countertops will be installed in a few days, but the walls already have a coat of primer on them. The process is underway and we’re really looking forward to it. One of the big additions for me is the new flat-screen high-definition television I set up this afternoon. Whether you’re upgrading your kitchen or your verification process, if you have a vision of where you want to be, the key is to do your planning up front, take it one step at a time, and don’t forget to enjoy the experience. The most important thing is to take that first step.

Respectfully submitted,
Tom Fitzpatrick
Editor, *Verification Horizons*

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Worlds Standards Day 2011

October 13th, 2011, by Dennis Brophy | Permalink | No Comments

Creating Confidence Globally

Today, 14 October 2011, is the day the world celebrates standards. The leadership of the IEC, ISO and ITU issued a message in support of it that clearly articulates the role standards play in safety, reliability, interoperability, their impact on business efficiency and more.

And from time-to-time, I have had the opportunity to join the celebration the American National Standards Institute (ANSI) in the United States hosted when the international community for electronic design automation specialists would gather in Washington, D.C. The highlight of the celebration in the United States is the presentation of the "Ronald Brown Standards Leadership Award" and the results from the Worlds Standards Day Paper Competition.

Ron Brown, Commerce Secretary in the United States until his untimely death in a plane crash in Croatia in 1996, is the namesake of the award. He was an inspiration to promote the role of standardization to eliminate global barriers to trade. ANSI honors this spirit annually, by naming their award after him. When this year's award recipient is announced, they will join a [long list](#) of other important people recognized as well.

The winner of the 2011 World Standards Day paper competition will also be announced. This year, ANSI selected the theme of "Advancing Safety and Sustainability Standards." Past year winners and their papers can be found [here](#). One of my favorite papers was the 1999 paper, *The Yin and Yang of Standards Development*. The paper juxtaposed formal standards development against that of consortia.

While I won't say one is right or wrong, I can say I offer leadership to the international bodies, like IEC, the formal bodies, like the IEEE and consortia like Accellera. If you have some take on this, I would be more than interested to hear.

For #electronic design automation, a good example of respecting the value of each of these is offered by [SystemVerilog](#). We know that SystemVerilog started as donations from many sources that became an Accellera standard. After a year of stabilization, it was transferred to the IEEE for




ABOUT VERIFICATION HORIZONS BLOG

This blog will provide an online forum to provide weekly updates on concepts, values, standards, methodologies and examples to assist with the understanding of what advanced functional verification technologies can do and how to most effectively apply them. We're looking forward to your comments and suggestions on the posts to make this a useful tool.

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#DENNISBROPHY TWEETS

- #Accellera Chair Shishpal Rajwat Talks About Roadmap for IP and System Design #Standards at IP-SOC 2011 <http://t.co/YfYDQ9z> # 19 hours ago
- Performance Counts: Acceleration of #SystemC and #TLM-2.0 Testbenches with Co-Emulation <http://t.co/ffuqjITSS> #semEDA # 2011/11/01

#DAVE_59 TWEETS

- Finished a review of papers for #DVCon, #QVM & #UVM are still hot topics, but so are #analog, #debug & #oviragedclosure. #Accellera # 2011/10/20
- #Mentor booth at #TSMC QIP FORUM <http://t.co/2ZjSfKyb> # 2011/10/19

LATEST POSTS

- Worlds Standards Day 2011
- VHS or Betamax?
- Verification Issues Take Center Stage
- New UVM Recipe-of-the-Month: Sequence Layering
- Combining Intelligent Testbench Automation with Constrained Random Testing
- Going from "Standards Development" to "Standards Practice"

TAGS

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- UVM (145)
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- acellera (140)
- functional verification (126)
- IEEE (120)
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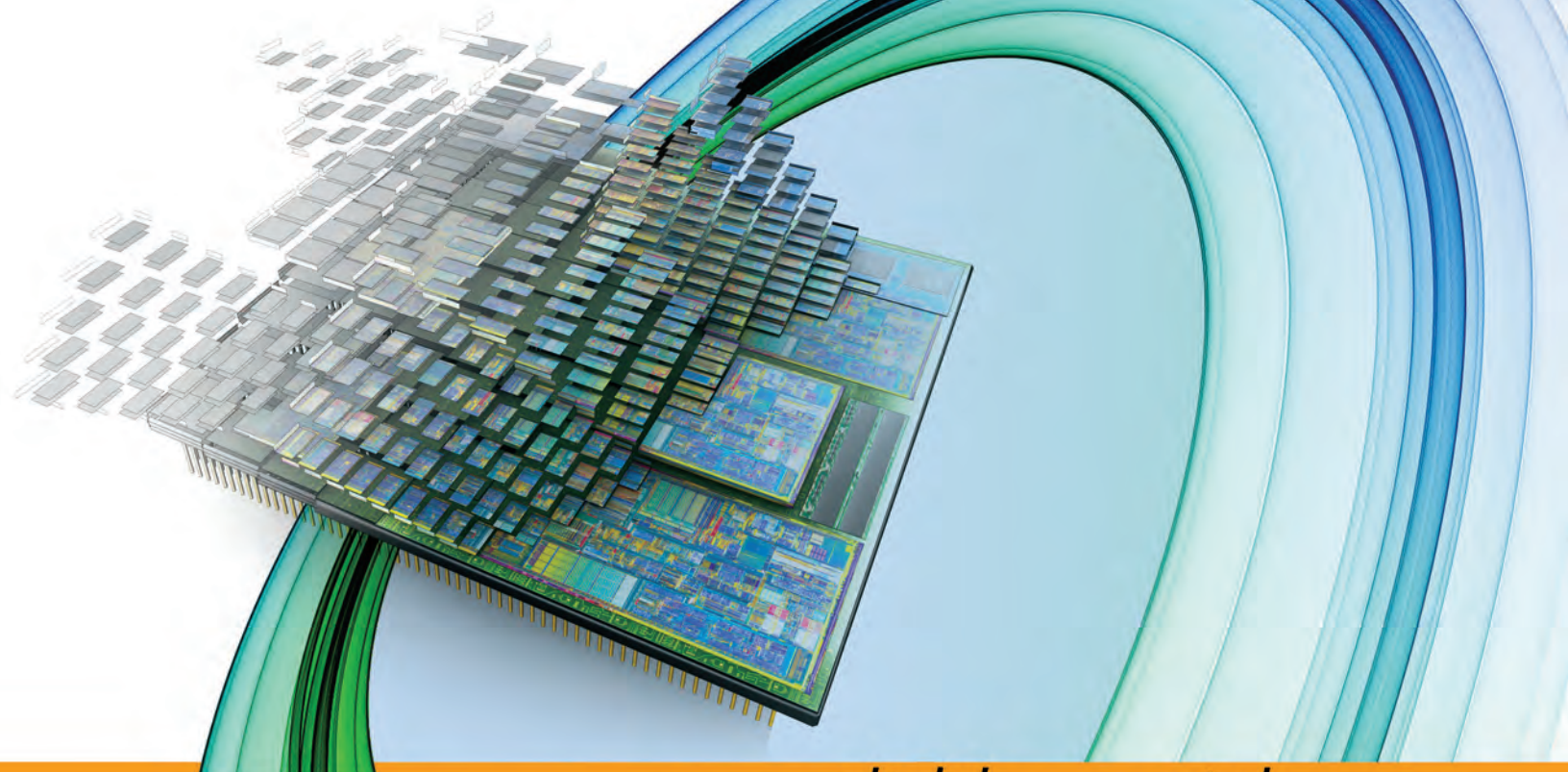
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- ARM SoC Design

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